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LOW PHASE NOISE LC VOLTAGE CONTROLLED OSCILLATOR: A REVIEW

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Abstract - The LC Voltage Controlled Oscillator is the most crucial part of the Phase Lock Loop that leads to produce a high system frequency in the range of GHz - RF band for the wireless Devices. The LC VCO – main block of PLL plays vital role in majority of applications in ISM frequency band - RF frequency band (Industrial, Scientific, Medical) like - IEEE 802.11a/b/g, Zigbee, front-end RF transceiver, - IEEE 802.15.4, Bluetooth etc. The overall performance and efficiency of these designs for applications depend upon the parameters and design methods of the LC Voltage - Oscillator. As a requirement to satisfy accuracy and efficiency constrains, new design techniques have been presented in this review paper to improve the features like phase noise, low power, FOM and frequency tuning range for new circuit design technique. In this era, different design methods have been used in LC VCO to improve performance parameters of LC VCO to achieve best results. Still research is going on to achieve more accurate results. The main objective of this review paper is to serve different design techniques of LC VCO to achieve low Phase Noise and low power including FOM in the frequency band of ISM. In the proposed Paper, the comparative analysis is presented for different design techniques of LC VCO with merits – demerits of all the features and concluding remarks in the field of ISM band applications.

Key Words: PLL, VCO, ISM Band, Current starved VCO, Power, LC Voltage Controlled Oscillator, Ring Oscillator, Phase Noise, FOM

1. INTRODUCTION

VLSI has become a cornerstone of modern technology, impacting various industries and enhancing the daily lives through increased computational connectivity, efficiency, and functionality. VLSI is a critical element of the semiconductor industry. VLSI technology enables the creation of complex integrated circuits (ICs) that power numerous electronic devices we rely on every day. From smart phones and tablets to laptops, smart watches, televisions, and even House-hold appliances 5, VLSI chips are at the core of these devices, providing processing power 6, memory, and other functionalities 3.

In these applications high system frequency in the range of RF - GHz is required for ISM band and microwave band 4. A PLL (phase locked loop) is widely used to generate and synchronies the high system frequency in these applications 30. Phase- locked loop can be used to achieve frequency synthesis and phase extraction and also to achieve an exact phase and Frequency relation between input frequency and generated system frequency 2. Phased lock loop is a control system that makes an output signal whose frequency is depends on the input phase difference 1.

The features including phase noise, power, FOM and system frequency should be included while designing the new technique to achieve better results. As a main crucial part of PLL, VCO need to design with all these parameters including reduced power supply and scaling is the challenging task for researchers 30.

The paper is organized as follows: Section II presents the Phase Lock Loop. Section III describes about the Voltage Controlled oscillator, types of VCO and the types of LC VCO. Section IV explains all preliminaries of VCO for phase noise generation in the oscillator with relative analysis among previous literature and section V gives conclusion of the survey with concluding remarks.

2. PHASE LOCK LOOP

Phase lock loop is widely used in the high speed data communication systems. So in the recent years, the design of low jitter PLL for the different application has become one of the greatest challenges in high performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power consumption and reduction in jitter of new VLSI circuits. Phase Locked Loop (PLLs) generates well- timed on-chip clocks for various applications such as clock-and-data recovery, clock multiplication and generation in microprocessor and frequency synthesizer 31.

As shown in Figure 1, the basic blocks of a PLL are: 1. PFD - Phase Frequency Detector 2.Charge Pump 3. Loop Filter - Low Pass Filter 4. VCO - Voltage Controlled Oscillator 5. Frequency Divider

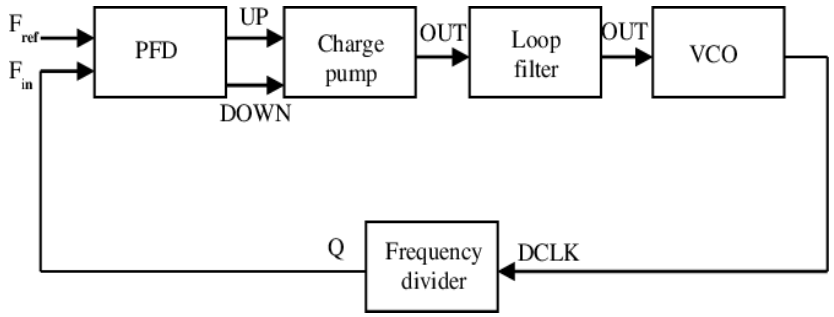

Fig.1. Block diagram of PLL

2.1 Phase Frequency Detector

The UP and DWN signals of the PFD depends on both the frequency and phase of the inputs. This category of phase detector is also termed a sequential phase detector. It performs the comparison of leading edges of Fref and Fin. When Fref leads rising edge of Fin the "UP" signal of the PFD goes high while the DWN signal is at ground. This causes the D'clock frequency to increase, having the effect of moving the edges close together and vice- versa. The PLL enters into lock mode when the frequency and phase of Fref and Fin is same and it is known as lock in range.

2.2 Charge Pump

The CP derives its name from the actuality that the phase detector (PD) output is applied to current source 'pulls' and "pumps" current into and out of the loop-filter according to width of Up and DWN signals.

2.3 Loop Filter - Low Pass Filter

The low-pass filter filter-out high- frequency noise and unwanted signals from the output-signal of the phase detector. The main purpose of the low-pass filter in PLL is it converts the current output from the CP into voltage which will be the input of oscillator. A well- designed low-pass filter minimizes noise and distortion, which allows the PLL to achieve a precise phase lock and maintain signal integrity.

2.4 Voltage Controlled Oscillator

Voltage Controlled Oscillator is the heart of Phase lock loop to generate stable and accurate output frequency. It is discussed in detail in Section III.

2.5 Frequency Divider

Frequency divider is a component that takes an input signal and produces an output signal whose frequency is a fraction of the input frequency.

3. VOLTAGE CONTROLLLED OSILLATOR

Over a decade, the rapid demand and work has been done on the Voltage controlled oscillator, the crucial part of the Phase Lock Loop is used to produce precise and steady system frequency. The output of low pass filter will be the input of VCO to generate System frequency. 29

Types of VCO: 1. Current-Starved VCO 2. LC VCO

3.1 Current starved VCO

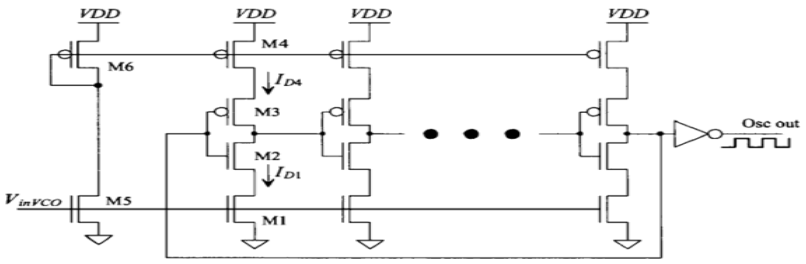

Fig.2. Current starved VCO

The current starved VCO is shown schematically in above figure2. Its operation is similar to the Ring oscillator. MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4 limit the current available to the inverter, M2 and M3. The MOSFETs M5 and M6 drain currents are the same and are set by the input control voltage. Current-starved VCO compared to an LC Voltage Oscillator is its generally higher phase noise. In the range of GHz-ISM freq. band applications, current starved, Ring 8 and LC VCO are commonly used. Compare to LC oscillator, Ring 9and current staved oscillators suffer more from high phase noise, so as a best choice, LC VCO is selected for majority applications 107. LC VCO is more attractive due to lower phase noise, power consumption and RMS jitter 1314. Although, higher area occupation is there compared to that of Ring oscillator. LC (inductor-capacitor) VCOs are commonly used in various processes due to several advantageous characteristics:

- **Tuning Range:** LC VCOs often offer a broader tuning range compared to other VCO topologies, where the frequency may need to be adjusted over a large span 12.
- **Frequency Stability:** LC-based VCOs can provide excellent frequency stability due to an LC tank circuit and once properly designed, it can offer a stable oscillation frequency.
- **Low Phase Noise:** Current-starved VCOs often exhibit increased noise levels compared to LC VCO due to the limited available current, impacting their frequency stability and overall performance in certain applications.
- **Integration and Miniaturization:** In integrated circuit (IC) design, space is often limited, and components need to be miniaturized. LC VCOs can be integrated into a smaller area because they typically require fewer components compared to other types of VCOs, making them advantageous in VLSI and IC designs.
- **Low power Consumption:** When designed efficiently, LC VCO can operate with low power, which is crucial in the battery operated systems and portable devices.
- **Ease of Design:** LC VCOs can be designed with relatively straightforward structures, making them more accessible for implementation in various integrated circuits.

3.2 LC Voltage Controlled Oscillator

The LC Voltage Controlled Oscillator is constructed with LC tank circuit to achieve resonance frequency, which will become the system frequency which the VCO is tuned. The main topologies of LC VCO are PMOS only, NMOS only and cross coupled complementary LC VCO 27. Each type of VCO has its best

features compared to other two with different parameters. In different literature, as per the requirement of features the correct selection of the topology is done.

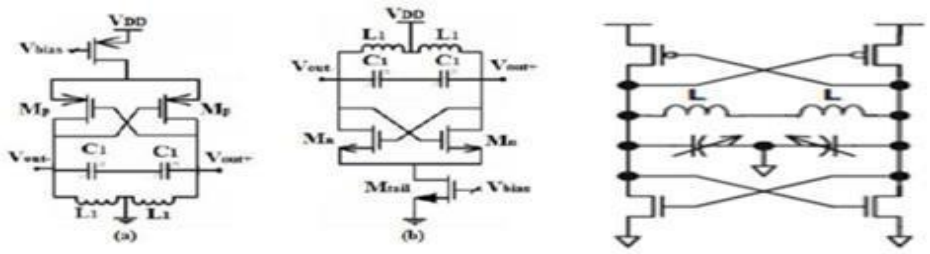

Fig.3. (a) PMOS topology 16 (b) MOS topology 16 (c) Complementary LC Oscillator 23

4. LC OSCILLATOR PRELIMINARIES

4.1 Oscillator Frequency and Tuning Range:

Higher frequencies and broader tuning ranges are the main desirable feature for versatile applications [2224]. The tuning rang and oscillator frequency at which it is tuned can be found by: [1112]

$$\text{Oscillator Frequency} = F_{LC} = \frac{1}{2\Pi\sqrt{LC}} = \frac{1}{2\Pi\sqrt{L(Cvar + Cpar + Cmos)}} \quad (1)$$

$$\text{Frequency Tuning range} = FTR = \frac{Cpar + Cvmax}{Cpar + Cvmin} \quad (2)$$

4.2 Phase Noise:

The overall performance of the VCO and PLL is depends upon the Phase noise. The theoretical calculation of the phase noise is [141522]:

$$L(\Delta w) = 10 \log\{ (1+(\frac{f0}{2Q\Delta w})^2)(1+\frac{w0}{\Delta w})(\frac{FkT}{2Pav}) + 2kTRk0/\Delta w^2 \quad (3)$$

4.3 Figure of Merit (FOM):

A higher FOM generally indicates a more balanced performance in terms of phase noise, power consumption, and offset frequency can be calculated 14.

$$FoM = L(\Delta w) + 10 \log [\frac{p}{1mw} (\frac{w0}{\Delta w})^2] \quad (4)$$

Where, $L(\Delta w)$ is the phase noise of oscillator, $w0$ is the oscillation frequency, Δw is the output offset - frequency , P is the DC power consumption.

4.4 Power Consumption:

Lower power consumption is preferable for many applications, especially in energy- sensitive or portable devices.

5. SURVEY OF DIFFERENT TECHNIQUES OF LC-VCO TO REDUCE PHASE NOISE

5.1 Top biasing with current mirror

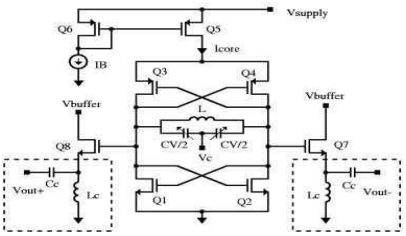

Fig.4. Top Biasing LC VCO with current mirror 23

The figure-4 shows the LC VCO tank circuit, which consists of 4 parts: an LC tank circuit, a source of negative transconductance (gm), a current source with output buffers. These components are off- chip as shown. The complementary topology is used to get low PN. The current source consists of a PMOS as shown in figure - Q5 and Q6- current mirror and the main core current of VCO - Icore is controlled by the external bias current (IB) through the current mirror. These Q5 –Q6 may affect the phase noise because it will add noise through the current source, but it is require integrating the circuit of PLL and remaining circuits. As shown, the complementary MOSFETs including Q1 and Q2- nMOS and Q3 and Q4 - pMOS, which set the VDC level of the output of VCO at VVCC /2. In the output buffers bias-tees and source followers are included. This will improve the bandwidth because of lower diffusion capacitance. The tank circuit- LC consists of an inductor (L) and two varactor capacitors (CV/2 and CV/2) to tune the frequency. The quality-factor of the LC-tank circuit is approx. equal to the parallel connected the QL- inductor Q and the QC - varactor Q. Generally, the Q of L is lower and so it dominant, actually on-chip inductors usually suffer from thin wiring levels and losses in the substrate. As a part of solution, proper layout is done to improve QL and by use of thick wiring levels or parallel multiple levels of wiring or higher resistivity substrate is used.

5.2 LC VCO with resonator technique

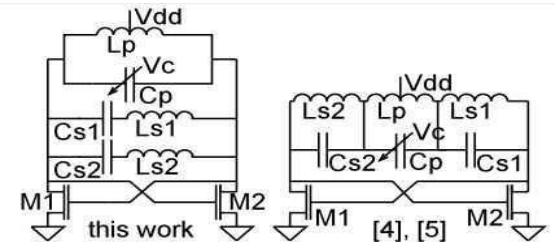

Fig.5. LC VCO with Resonator Technique 26

The proposed resonator design employs all parallel filter topology. To get lower phase noise, the proposed resonator design is introduced. The design of the proposed resonator is shown in left side of the above figure 5 where Lp, Cp are the LC-tank and serially connected resonators composed of the Ls1, Cs1 and Ls2, Cs2 respectively. All-parallel topology has lower serial resistance and thus larger Q-factor than the tuned harmonics topology in the right side of the above figure 5, although both topologies are exhibiting the same pattern of the resonances. In the simulation, the foundry models has used for the on-chip spiral inductor Lp and MIM capacitors Cp, Cs1, Cs2 and 3-stage RL-ladder NW was used to simulate the Ls1 and Ls2, because Ls1 and Ls2 was implemented using the 20 um thick bonding wires. The oscillation generated in the resonance 3, resonances 2 and

4 lowers impedance around it, which reduces total noise voltage. Resonances 1 and 5 are undesired, because oscillation can happen on them instead of the desired oscillation mode.

5.3 LC-VCO with Active Inductor Technique

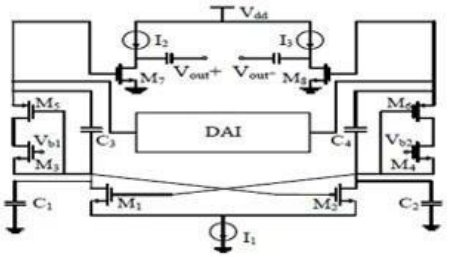

Fig.6. LC VCO with Active Inductor Technique 25

In the literature 25, to solve the problem of higher area occupancy, active Inductor is used in the LC oscillator, which is best replacement of off chip inductor.
In this 25 paper, the differential active inductor with the technique to reduce phase noise is used to achieve -117.2dBc/Hz PN at 1MHz offset frequency. Complementary topology of LC oscillator is used with extra capacitors, current bias source and MOSFETs are intended to obtain higher output power. Lower power consumption and enhanced PN has been achieved, but as a cost of active inductor technique, which consumes higher power consumption to acquire less area.

5.4 Top biasing with current mirror

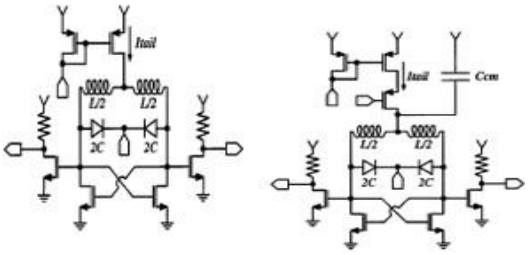

Fig.7. Top biasing LC VCO with current mirror technique 19

The proposed paper 19, cascode tail current technique with top biasing is presented. In proposed literature, two nMOS only LC oscillators are proposed with top biasing technique. Ccore is connected parallel to current mirror circuit and extra MOSFET in series. The ckt is cascode at the common node with the top biasing circuit of tail biasing. This technique removes extra common mode variations, because of the key parameter of VCO technique, the overdrive voltage Vgs -Vt, of nMOS. The correct choice of this voltage is required for good output amplitude, tolerable flicker noise, and power and generated parasitic of the nMOS. In the proposed technique by keeping gm of nMOS constant and considering trade-off, the value of 1/f3 phase noise factor is selected. As a trade-off, the correct Vgs – Vt is also selected. The proposed design gives lower phase noise by reduction in 1/f3 -flicker noise up conversion. This is achieved by tail current source tech. and disadvantage of extra supply voltage is required for biasing.

In 20 proposed technique, tail biasing is applied at common node with external current source to decrease the PN. As proposed tech. shows direct connection of current source at the node of nMOS cross coupled pair, supplies direct current in the oscillator with correct quantity and at correct time. This will result in reduced ISF and reduces the total phase noise.

5.5 Tail Biasing LC VCO with current source

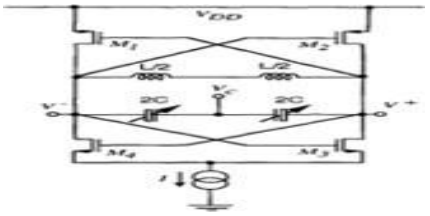

Fig. 8 Tail biasing LC VCO with current source [20]

5.6 Tail Biasing LC VCO with Auxiliary gm class B

A proposed complementary class-C VCO; by Fanori etal, exploits a PMOS – NMOS complementary pair operating in class-C Mode to enhance the output swing and ensures a fast start-up.

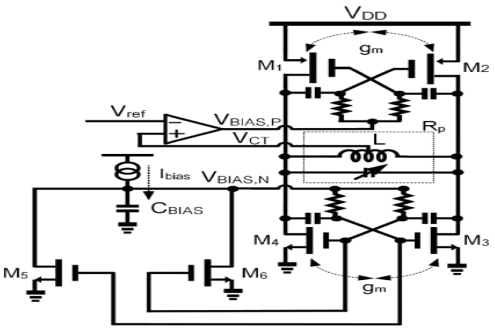

Fig.9. Tail biasing LC-VCO with Auxiliary gm-class B 28

In Proposed design in 28 as shown in figure 9, has extra resistors and capacitor connected with tail biasing - pMOS and the circuit of class B- auxiliary gm. The purpose of resistors are to get direct Vbias for early start of oscillation and the capacitor as a capacitive degeneration component to achieve lower phase noise. The proposed technique results in good PN but requirement of extra circuit increases area.

6. CONCLUSIONS

This review paper presents the survey analysis of LC VCO with all the features to achieve low phase noise design Techniques. From this survey, the supply is reduced from 2V in 2000 to 0.5V in 2010 and scaling down of technology at 0.18 µm. Frequency and Tuning Range of the oscillators frequencies have varied from 2GHz to 6.77GHz, with tuning ranges becoming broader in more recent designs, reaching from 1.126GHz to 2.713GHz. There's a consistent effort to reduce phase noise across the years, progressing from around -120dBc/Hz in early designs to as low as -131.3dBc/Hz in the 2010 design, signifying enhanced signal quality. Power efficiency has seen improvements as well. The earliest designs consumed power around 1.5mW to 13.6mW, but later designs have shown a tendency towards lower power consumption, reaching as low as 1.6mW to 1.73mW. Best FOM is the 2010 design by Oleg N. leads with the highest FOM of 196.3, suggesting a well-balanced performance in terms of phase noise, power, and offset frequency. Lowest Power Consumption is of 2003 designed by J. Kim et al. consumes the least power at 1.5mW, indicating good efficiency.

Considering these parameters collectively, the 2010 design by Oleg N. stands out as the best-rounded oscillator, excelling in frequency, phase noise, FOM, and still maintaining relatively low power consumption. However, the choice of the "best" LC voltage controlled oscillator depends on the specific requirements of the application, as different designs might excel in different areas. The 2019 and 2003 design also shows hopeful performance with improved tuning range and comparable power consumption. The techniques surveyed in this paper required for the design of LC oscillator to improve phase noise are highly depending upon the requirements of major parameters and application.

YEAR	AUTHOR	Supply	Tech. (µm)	Freq. (GHz)	TUNING RANGE(GHz)	PHASE NOISE	OFFSET Freq.	FOM	Power (mw)
2000	Bram D. et al. 19	1.8V	0.65	2	1.79 – 2	-125dBc/Hz	600kHz	-	-
2000	F. Svelto et al.20	2V	0.35	2.12	1.83 – 2.45	-120.5dBc/Hz	600kHz	187.5	-
2003	J. Kim et al. 23	1.5V	0.18	2.55	–	-119.2dBc/Hz	1MHz	185.57	1.5
2018	Yin Z. et al. 25	1.8V	0.18	-	1.126 – 2.713	-117.2dBc/Hz	1MHz	188.78	13.6
2010	Oleg N. et al. 26	0.5V	0.18	6.77	–	-131.3dBc/Hz	3MHz	196.3	1.6
2019	Pravinah S.et al.28	1.2V	0.18	2.4	2.2 – 2.9	-120dBc/Hz	1MHz	185.4	1.73

Table 1: Comparative analysis of LC Voltage Controlled Oscillator with parameters

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